

Notice of Allowability

Application No.

10/042,098

Examiner

Erin M. File

Applicant(s)

DRERUP ET AL.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 1/7/2002.
2. ☒ The allowed claim(s) is/are 1-20.
3. ☒ The drawings filed on 07 January 2002 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 1/7/2002
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date 06032005.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Anthony England, Reg. No. 35,129 on June 3, 2005.

2. The application has been amended as follows:

Claim 6, The method of claim 5, wherein step d) further comprises the steps of: latching signals for the edge counter, including the count signal from the state machine and the detected level signal from the edge detector, responsive to the certain edge of the first clock for each cycle of logic operations; resetting the edge counter to a certain middle value during a logic cycle as indicated by the count signal of the state machine. incrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has not reached a high or low limit, and the detected level output by edge detector is high; decrementing the edge counter during the logic cycle if the count signal indicates the state machine requires counting, and the edge counter has not reached a high or low limit, and the detected level output by edge detector is low; holding the edge counter during the logic cycle if

the count signal indicates the state machine requires counting, and the edge counter has reached a high or low limit

Claim 7, The method of claim 3, wherein step d) further comprises the steps of: latching signals for the flip timer, including the count signal from the state machine, responsive to a certain edge of the first clock for each cycle of logic operations; resetting the flip timer to a certain starting value during a logic cycle if the count signal indicates the state machine does not require counting down; decrementing the flip timer during a logic cycle if the count signal indicates the state machine requires counting down; and holding the flip timer during a logic cycle if the count signal indicates the state machine requires counting down and the flip timer has expired.

Claim 8, The method of claim 3, wherein the second logic includes a synchronizer, and step d) further comprises the steps of: latching certain signals for the synchronizer, including the flip signal from the state machine, responsive to a certain edge of the second clock for each cycle of logic operations; and asserting a derived clock gate output signal for the synchronizer if the flip signal indicates that the state machine indicates a phase adjustment.

Claim 14, The apparatus of claim 12, wherein the first logic includes an edge detector, and repeatedly sampling the third clock using the first clock comprises ~~outputting~~ outputting by the edge detector, as a detected level signal, the state of the third clock,

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wherein the third clock state is latched responsive to each instance of a certain edge of the first clock.

3. The following is an examiner's statement of reasons for allowance:

The detailed limitations of independent claims 1, 10, and 19, particularly the steps of detecting relative phase relations of the first and third clock signals repeatedly by the first logic circuitry; and altering the phase of the third clock signal responsive to an accumulation of the phase relation detecting, cannot be found in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin File

EF

6/3/2005


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